Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listings of Claims:

1. (original) A non-volatile semiconductor memory device comprising any one of a current supply control transistor disposed between a voltage source and a non-volatile memory cell and connected serially to said voltage source and said non-volatile memory cell, and a current absorption control transistor disposed between said non-volatile memory cell and a reference potential and connected serially to said non-volatile memory cell and said reference potential,

wherein said current supply control transistor or said current absorption control transistor is operated in a current saturation area denoted by current-voltage characteristics, thereby controlling a current that flows in said non-volatile memory cell at data writing.

2. (original) A non-volatile semiconductor memory device comprising: a current supply control transistor

disposed between a voltage source and a non-volatile memory cell and connected serially to said voltage source and said non-volatile memory cell; and a current absorption control transistor disposed between said non-volatile memory cell and a reference potential and connected serially to said non-volatile memory cell and said reference potential,

wherein both of said current supply control transistor and said current absorption control transistor are operated in a current saturation area denoted by current-voltage characteristics, thereby controlling a current that flows in said non-volatile memory cell at data writing.

3. (original) The non-volatile semiconductor memory device according to claim 2,

wherein a difference between a current that flows in said current supply control transistor and a current that flows in said current absorption control transistor is used as a writing current for said non-volatile memory cell.

4. (currently amended) The non-volatile semiconductor memory device according to claim 2 ~~or 3~~, further comprising:

a trimming part that includes a trimming information storage part for storing current trimming information and a decoder circuit for decoding said current trimming information stored in said trimming information storage part to output a voltage,

wherein said trimming part generates a voltage to be applied to the gate of each of said current supply control transistor and said current absorption control transistor based on said current trimming information.

5. (original) The non-volatile semiconductor memory device according to claim 1, further comprising:

a trimming part that includes a trimming information storage part for storing current trimming information, and a decoder circuit for decoding said current trimming information stored in said trimming storage part to output a voltage,

wherein said trimming part generates a voltage to be applied to the gate of either said current supply control transistor or said current absorption control transistor based on said current trimming information.

6. (currently amended) The non-volatile semiconductor memory device according to ~~any of claims~~ claim 1 ~~to 5~~,

wherein said trimming information storage part stores trimming information related to a power supply circuit.

7. (currently amended) The non-volatile semiconductor memory device according to ~~any of claims~~ claim 1 ~~to 6~~,

wherein said non-volatile memory cell includes two transistors, each having a selector gate and a memory gate.

8. (original) The non-volatile semiconductor memory device according to claim 7,

wherein the gate of each of said current supply control transistor and said current absorption control transistor is longer than that of said selector gate of said non-volatile memory cell.

9. (original) A semiconductor integrated circuit device including a non-volatile storage part and a central processing unit,

said central processing unit can execute a predetermined processing and instruct said non-volatile storage part to make an operation, and said non-volatile

storage part includes a plurality of non-volatile memory cells for storing information,

wherein said non-volatile storage part includes any one of a current supply control transistor disposed between a voltage source and a non-volatile memory cell and connected serially to said voltage source and said non-volatile memory cell, and a current absorption control transistor disposed between said non-volatile memory cell and a reference potential and connected serially to said non-volatile memory cell and said reference potential, and

wherein said current supply control transistor or said current absorption control transistor is operated in a current saturation area denoted by current-voltage characteristics, thereby controlling a current that flows in said non-volatile memory cell at data writing.

10. (original) A semiconductor integrated circuit device including a non-volatile storage part and a central processing unit,

wherein said central processing unit can execute a predetermined processing and instruct said non-volatile storage part to make an operation, and said non-volatile

storage part includes a plurality of non-volatile memory cells for storing information,

wherein said non-volatile storage part includes: a current supply control transistor disposed between a voltage source and a non-volatile memory cell and connected serially to said voltage source and said non-volatile memory cell; and a current absorption control transistor disposed between said non-volatile memory cell and a reference potential and connected serially to said non-volatile memory cell and said reference potential, and

wherein said current supply control transistor and said current absorption control transistor are operated in a current saturation area denoted by current-voltage characteristics, thereby controlling a current that flows in said non-volatile memory cell at data writing.

11. (original) The semiconductor integrated circuit device according to claim 10,

wherein a difference between a current that flows in said current supply control transistor and a current that flows in said current absorption control transistor is used as a writing current for said non-volatile memory cell.

12. (currently amended) The semiconductor integrated circuit device according to claim 10 ~~or 11~~, further comprising:

a trimming part that includes a trimming information storage part for storing current trimming information, and a decoder circuit for decoding said current trimming information stored in said trimming information storage part to output a voltage,

wherein said trimming part generates a voltage to be applied to the gate of each of said current supply control transistor and said current absorption control transistor according to said current trimming information.

13. (original) The semiconductor integrated circuit device according to claim 9, further comprising:

a trimming part that includes a trimming information storage part for storing current trimming information, and a decoder circuit for decoding said current trimming information stored in said trimming information storage part to output a voltage,

wherein said trimming part generates a voltage to be applied to the gate of either said current supply control

transistor or said current absorption control transistor according to said current trimming information.

14. (currently amended) The semiconductor integrated circuit device according to ~~any of claims~~ claim 9 ~~to 13~~,

wherein said trimming information storage part stores trimming information related to said power supply circuit.

15. (currently amended) The semiconductor integrated circuit device according to ~~any of claims~~ claim 9 ~~to 14~~,

wherein said non-volatile memory cell includes two transistors, each having a selector gate and a memory gate.

16. (original) The semiconductor integrated circuit device according to claim 15,

wherein the gate of each of said current supply control transistor and said current absorption control transistor is longer than that of said selector gate of said non-volatile memory cell.

17. (original) A non-volatile semiconductor memory device including any one of a current supply control transistor disposed between a voltage source and a non-

volatile memory cell and connected serially to said voltage source and said non-volatile memory cell, and a current absorption control transistor disposed between said non-volatile memory cell and a reference potential and connected serially to said non-volatile memory cell and said reference potential,

wherein said non-volatile memory cell includes a control transistor and a memory transistor having a charge storage area, and applies a first voltage to the control gate of said control transistor and a second voltage to the control gate of said memory transistor, and

wherein said current supply control transistor or said current absorption control transistor is operated in a current saturation area denoted by current-voltage characteristics, thereby controlling a current that flows in said non-volatile memory cell at data writing, and selectively applying either a third voltage lower than said second voltage or a fourth voltage lower than said third voltage to the control gate of said control transistor as said first voltage selectively.

18. (original) The non-volatile semiconductor memory device according to claim 17, further including a circuit

for generating said first voltage to be applied to the control gate of said control transistor,

wherein said circuit outputs either said third voltage or said fourth voltage as said first voltage.

19. (original) The non-volatile semiconductor memory device according to claim 18, further including a register for storing information used to determine which of said third voltage and said fourth voltage should be output as said first voltage.

20. (original) The non-volatile semiconductor memory device according to claim 18,

wherein in said circuit, which of said third voltage and said fourth voltage should be output as said first voltage is determined according to an instruction that includes information used for such output voltage determination.